

### **Amendments to the Claims**

1. (*Currently Amended*) A test module for testing the susceptibility of an integrated circuit design to latch-up, the test module ~~comprising~~ comprising:  
\_\_\_\_\_ a plurality of test blocks (30), connected in parallel, each test block ~~comprising~~ including an injector block (12) for applying a stress current or voltage to the respective test block (30), and  
\_\_\_\_\_ a plurality of sensor blocks (13) located at successively increasing distances from the respective injector block (12), each sensor block (13) ~~comprising~~ including a PNPN latch-up test structure.
2. (*Currently Amended*) ~~A test module according to claim 1,~~ The test module as recited in claim 1, wherein each test block (30) is connected to a bondpad (11), said stress current or voltage being applied to said injector (12) via said bondpad (11).
3. (*Currently Amended*) ~~A test module according to claim 1 or claim 2,~~ The test module as recited in claim 1, wherein said injector blocks (12) are connected between first and second supply lines (14,15).
4. (*Currently Amended*) ~~A test module according to any one of claims 1 to 3,~~ The test module as recited in claim 1, wherein contacts (5,6) of said sensor blocks (13) are connected between third and fourth supply lines (18,19), different from said first and second supply lines (14,15).
5. (*Currently Amended*) ~~A test module according to any one of the preceding claims~~ The test module as recited in claim 1, wherein each PNPN latch-up structure ~~comprises~~ includes an N<sup>+</sup> and a P<sup>+</sup> hot-active (7,8), which hot-actives (7,8) are connected to respective probe sensor lines (16,17).

6. (*Currently Amended*) ~~A test module according to any one of the preceding claims,~~ The test module as recited in claim 1, wherein heating means (20) is provided in respect of said PNP latch-up test structures.

7. (*Currently Amended*) A test module according to claim 6, wherein said heating means comprise polysilicon rings (20) located around respective PNP latch-up test structures.

8. (*Currently Amended*) A method of testing the susceptibility of an integrated circuit design to latch-up, the method ~~comprising~~ comprising:  
\_\_\_\_\_ providing a test module comprising a plurality of test blocks (30), connected in parallel, each test block (30) ~~comprising~~ including,  
\_\_\_\_\_ an injector block (12) for applying a stress current or voltage to the respective test block (30), and  
\_\_\_\_\_ a plurality of sensor blocks (13) located at successively increasing distances from the respective injector block (12), each sensor block (30) ~~comprising~~ including a PNP latch-up test structure,  
\_\_\_\_\_ ~~the method further comprising~~ applying a stress current or voltage to one or more of the injector blocks (12), and  
\_\_\_\_\_ obtaining resultant current measurements at one or more of the respective sensor blocks (13).

9. (*Currently Amended*) ~~A method according to claim 8,~~ The method as recited in claim 8, further comprising,  
\_\_\_\_\_ disconnecting said sensor blocks (13) during application of said stress current or voltage to one or more of said injector blocks (12), and  
\_\_\_\_\_ obtaining current measurements at said injector blocks (12) to determine the susceptibility thereof to latch-up.

10. (*Currently Amended*) ~~A method according to claim 8 or claim 9,~~ The method as recited in claim 8, wherein an injector block (12) or a sensor block (13) is determined to

be susceptible to latch-up if a current measurement ~~thereat~~ therein exceeds a predetermined threshold.

11. (*Currently Amended*) ~~A method according to any one of claims 8 to 10,~~ The method as recited in claim 8, wherein sequential current measurements are obtained at each PNP latch-up test structure of a sensor block (13).

12. (*Currently Amended*) ~~A method according to any one of claims 8 to 11,~~ The method as recited in claim 8, wherein each injector block (12) and each sensor block (13) can be independently biased.

13. (*Currently Amended*) ~~A method according to claim 12,~~ The method as recited in claim 12, wherein each PNP latch-up test structure can be biased independently.